IN THE SPECIFICATION:

(1) The paragraph from page 1, line 7 to page 1, line 15 has been amended as follows:

The present invention relates to ~~a~~ test equipment for a function test in which output data output from an LSI as a device under test is compared with predetermined expectation value data to judge whether or not the LSI to be measured is failure, a jitter analyzer for analyzing a jitter of a clock or output data of an LSI to be measured which is a function test object, and a phase difference detector which detects a phase difference between a clock and output data of an LSI to be measured.

(2) The paragraph from page 1, line 16 to page 1, line 28 has been amended as follows:

The present invention relates particularly to ~~a~~ test equipment, in which a source synchronous circuit capable of acquiring a clock and output data output from an LSI to be measured as level data in a time series; in which a clock signal output from the LSI to be measured is accordingly usable as a timing signal to take in the output data of the LSI to be measured; which is capable of taking in the output data at a signal change point synchronized with a jitter; which is capable of obtaining a correct test result without being influenced by the jitter; and which is suitable for a

function test of a high-rate LSI having a data rate exceeding, for example, 1 GHz.

(3) The paragraph from page 2, line 9 to page 2, line 17 has been amended as follows:

In general, ~~a~~ test equipment to perform a function test of an LSI (hereinafter referred to as "LSI tester") inputs a predetermined test pattern signal into an LSI to be measured which is an object to be tested (device under test: DUT), compares output data output from the LSI to be measured with a predetermined expectation value pattern signal, and judges agreement/disagreement to detect/judge whether or not the LSI to be measured is failure.

(4) The paragraph from page 2, line 18 to page 2, line 20 has been amended as follows:

~~A conventional~~ Conventional test equipment for an LSI to be measured will be described hereinafter with reference to FIG. 10.

(5) The paragraph from page 3, line 3 to page 3, line 8 has been amended as follows:

In the conventional test equipment for the LSI to be measured constituted in this manner, first a predetermined test pattern signal is input to the LSI to be measured 101 from a pattern generation unit (not shown), and a ~~predetermined~~ signal responsive to the test pattern signal is output as the output data from the LSI to be measured 101.

(6) The paragraph from page 4, line 7 to page 4, line 17 has been amended as follows:

The fluctuation of the acquired data by the jitter will be described with reference to FIG. 11. As shown in ~~the figure (a)~~ FIG. 11(a), the output data of the LSI to be measured has the jitter with a width in a certain range, and a change point (rising or falling edge) of the output data shifts by the jitter width. Therefore, when the output data having this jitter is taken in at the fixed strobe, as shown in ~~the figure (b)~~ FIG. 11(b), for example, the acquired data is "H" in case of "output data 1" ~~(FIG. 11(a))~~, but the data is "L" in case of "output data 2" ~~(FIG. 11(b))~~.

(7) The paragraph from page 4, line 18 to page 4, line 23 has been amended as follows:

Therefore, in the conventional test equipment which acquires the output data by the fixed strobe, the data which is originally the same fluctuates by an influence of jitter, and a problem has occurred that correct test or judgment is difficult. Especially, the influence of the jitter is ~~remarkable in a speeded up~~ a serious problem for a high speed LSI.

(8) The paragraph from page 4, line 24 to page 5, line 9 has been amended as follows:

It is to be noted that to measure/analyze the jitter of the LSI to be measured, the output data of the LSI to be

measured has heretofore been measured by jitter measurement units such as an oscilloscope by repeating the measuring process a plurality of times, and a jitter amount, a distribution of jitters and the like have been analyzed based on measurement results. However, in the conventional jitter analysis using a jitter measurement unit, there is a possibility that an error is generated in the operation of the oscilloscope or the like. It is difficult to analyze the jitter with high precision. Moreover, an operation of acquiring and measuring a large number of data is complicated, and a problem that the jitter analysis requires much time and labor has been pointed out. Especially in the ~~speeded up~~ high speed LSI, such difficulty in the jitter analysis has been ~~remarkable~~ a serious problem.

(9) The paragraph from page 6, line 8 to page 6, line 22 has been amended as follows:

That is, the present invention has been proposed to solve the problem ~~owned by~~ involved in the above-described conventional technique, and an object is to provide ~~a~~ test equipment for an LSI as a device under test, in which a source synchronous circuit for outputting a clock and output data ~~output~~ from the LSI to be measured as level data in a time series is disposed, so that a clock signal output from the LSI to be measured is usable as a timing signal for acquiring the output data of the LSI to be measured and which is capable of

taking in the output data at a signal change point synchronized with a jitter and which is capable of obtaining a correct test result without being influenced by the jitter and which is suitable for a function test of a high-rate LSI having a data rate exceeding, for example, 1 GHz.

(10) The paragraph from page 7, line 6 to page 7, line 27 has been amended as follows:

To achieve the above-described objects, first, according to the present invention, ~~a~~ test equipment for an LSI to be measured ~~is a test equipment which~~ compares an output signal ~~output~~ from the LSI to be measured ~~as data to be measured~~ with predetermined expectation value data to judge whether or not the LSI to be measured is failure, and comprises: a first LSI tester which inputs a first signal output from the LSI to be measured and which acquires the first signal by a plurality of strobes having a certain timing interval to output level data in a time series; a second LSI tester which inputs a second signal output from the LSI to be measured and which acquires the second signal by a plurality of strobes having a certain timing interval to output level data in a time series; and a selection circuit which is disposed in at least one of the first and second LSI testers and which inputs the level data of the time series output from the first and second LSI testers to select the second signal input into the second LSI tester at a timing of the first signal input into the first

LSI tester and which outputs the second signal as the data to be measured of the LSI to be measured.

(11) The paragraph from page 7, line 28 to page 8, line 3 has been amended as follows:

According to the test equipment for the LSI to be measured of the present invention constituted in this manner, since the source synchronous circuit is disposed ~~according to the present invention~~, the clock and output data output from the LSI to be measured can be acquired as the level data of the time series.

(12) The paragraph from page 8, line 11 to page 8, line 20 has been amended as follows:

Accordingly, even when the signal change points ~~rising~~ (rising edge or falling edge) of the clock and output data of the LSI to be measured fluctuate by the jitters, it is possible to take in the output data at the edge timing of the clock which has fluctuated. Therefore, in the test equipment according to the present invention, the output data of the LSI to be measured can be acquired at a timing which fluctuates in accordance with the jitter, and a correct test result can always be obtained without being influenced by the jitter.

(13) The paragraph from page 9, line 6 to page 9, line 29 has been amended as follows:

Moreover, ~~concretely,~~ in the present invention, the first LSI tester comprises a first time interpolator including: a

sequential circuit which inputs a clock output from the LSI to be measured; a delay circuit which successively inputs a strobe delayed at a certain timing interval into the sequential circuit to output the level data of the time series from the sequential circuit; and an encoder which inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating an edge timing of the clock of the LSI to be measured to output the data. The second LSI tester comprises a second time interpolator including: a sequential circuit which inputs the output data ~~output~~ from the LSI to be measured; and a delay circuit which successively inputs the strobe delayed at a certain timing interval into the sequential circuit and which allows the sequential circuit to output the level data of the time series. The selection circuit comprises a selector which selects one data from the level data of the time series input from the second time interpolator using the level data of the time series coded by the first time interpolator as a selection signal to output the data to be measured of the LSI to be measured.

(14) The paragraph from page 9, line 30 to page 10, line 10 has been amended as follows:

According to the test equipment for the LSI to be measured of the present invention constituted in this manner, the first and second LSI testers and selection circuit

constituting the source synchronous circuit can be easily ~~constituted~~ established by using existing means such as the ~~order~~ sequential or delay circuit, encoder, and selector. Accordingly, the LSI tester comprising the source synchronous circuit according to the present invention can be realized by a simple constitution without complicating or enlarging the LSI tester or increasing a cost.

(15) The paragraph from page 10, line 11 to page 10, line 22 has been amended as follows:

Moreover, according to the source synchronous circuit constituted in this manner, the number of a plurality of sequential circuits and a delay amount of the delay circuit can be changed, and a bit width (the number of sequential circuits) or resolution (delay amount of the delay circuit) of the level data of the time series in the first and second time interpolators can be set to ~~an optional value~~ desired values. Accordingly, various settings are possible in accordance with a data rate, jitter width and the like, and it is possible to realize an LSI tester which is capable of coping with any LSI ~~and which has~~ while having high versatility and convenience.

(16) The paragraph from page 11, line 18 to page 11, line 22 has been amended as follows:

Furthermore, the present invention includes a ~~constitution comprising~~ a bus which is connected to the first and second LSI testers and which distributes data output from

the first and second LSI testers to a predetermined selection circuit.

(17) The paragraph from page 12, line 9 to page 12, line 21 has been amended as follows:

Next, a jitter analyzer for an LSI to be measured of the present invention ~~is a jitter analyzer which~~ acquires/analyzes ~~a~~ distribution of jitters of an output signal ~~output~~ from the LSI to be measured, and comprises: a first LSI tester which inputs the output signal ~~output~~ from the LSI to be measured and which acquires the output signal by a plurality of strobes having certain timing intervals to output level data in a time series; and jitter distribution analysis means for inputting the level data of the time series output from the first LSI tester to acquire the timing of the output signal input into the first LSI tester and for outputting the distribution of jitters of the output signal.

(18) The paragraph from page 13, line 10 to page 13, line 21 has been amended as follows:

Moreover, ~~concretely,~~ in the present invention, the first LSI tester comprises a time interpolator including: a sequential circuit which inputs an output signal ~~output~~ from the LSI to be measured; a delay circuit which successively inputs strobes delayed at certain timing intervals into the sequential circuit and which allows the sequential circuit to output the level data of the time series; and an encoder which

inputs the level data of the time series output from the sequential circuit and which encodes the level data into timing data indicating the edge timing of the output signal of the LSI to be measured to output the timing data.

(19) The paragraph from page 13, line 22 to page 14, line 1 has been amended as follows:

According to the jitter analyzer of the LSI to be measured of the present invention constituted in this manner, the first LSI tester constituting the source synchronous circuit can be easily ~~constituted~~ established by using the existing means such as the ~~order~~ sequential or delay circuit, and encoder. Accordingly, the jitter analyzer using the source synchronous circuit according to the present invention can be realized by a simple constitution without complicating or enlarging the jitter analyzer or increasing the cost.

(20) The paragraph from page 14, line 2 to page 14, line 14 has been amended as follows:

Moreover, according to the source synchronous circuit constituted in this manner, the number of a plurality of sequential circuits, and the delay amount of the delay circuit can be changed, and the bit width (the number of sequential circuits) or resolution (the delay amount of the delay circuit) of the level data of the time series in the time interpolator can be set to ~~an optional value~~ desired values. Accordingly, various settings are possible in accordance with

the data rate, jitter width and the like, and it is possible to realize a jitter analyzer which is capable of coping with any LSI ~~and which has~~ while having high versatility and convenience.

(21) The paragraph from page 15, line 16 to page 15, line 25 has been amended as follows:

Moreover, in the present invention, the jitter distribution analysis means comprises: a decoder which inputs the timing data output from the encoder and which decodes the timing data into the level data of the time series to output the level data; and a plurality of counters which count the output signals of the decoder for each output terminal, and is constituted to acquire ~~a~~ distribution of edge timings of the output signals input into the first LSI tester from a plurality of data output from the counter.

(22) The paragraph from page 16, line 19 to page 17, line 8 has been amended as follows:

Furthermore, a phase difference detector for an LSI to be measured of the present invention ~~is a phase difference detector which~~ detects a phase difference between first and second signals output from the LSI to be measured, and comprises: a first LSI tester which inputs a first signal output from the LSI to be measured and which acquires the first signal as data by a plurality of strobes having a certain timing interval to output level data in a time series;

a second LSI tester which inputs a second signal output from the LSI to be measured and which acquires the second signal as data by a plurality of strobes having a certain timing interval to output level data in a time series; and a phase difference detection circuit which is disposed in at least one of the first and second LSI testers and which inputs the level data of the time series output from the first and second LSI testers to calculate a difference between a timing of the first signal input into the first LSI tester and that of the second signal input into the second LSI tester and which outputs the phase difference.

(23) The paragraph from page 21, line 26 to page 21, line 28 has been amended as follows:

FIG. 1 is a block diagram showing a constitution of a first embodiment of ~~a~~ test equipment for an LSI to be measured according to the present invention;

(24) The paragraph from page 21, line 29 to page 22, line 3 has been amended as follows:

~~FIG. 2 is a signal diagram~~ FIGS. 2(a) and 2(b) are signal diagrams showing an operation for acquiring output data at an edge timing of a clock of the LSI to be measured in the first embodiment of the test equipment for the LSI to be measured according to the present invention;

(25) The paragraph from page 22, line 23 to page 22, line 27 has been amended as follows:

~~FIG. 8 is a signal diagram~~ FIGS. 8(a) and 8(b) are signal diagrams showing an operation for acquiring a phase difference between the clock and output data of the LSI to be measured in the first embodiment of the phase difference detector for the LSI to be measured according to the present invention;

(26) The paragraph from page 23, line 2 to page 23, line 4 has been amended as follows:

FIG. 10 is a block diagram showing a constitution of ~~a~~ conventional test equipment for an LSI to be measured; and

(27) The paragraph from page 23, line 5 to page 23, line 9 has been amended as follows:

~~FIG. 11 is a signal diagram~~ FIGS. 11(a) and 11(b) are signal diagrams showing the output data of the LSI to be measured in the conventional test equipment for the LSI to be measured, ~~(a)~~ FIG. 11(a) shows a jitter of output data, and ~~(b)~~ FIG. 11(b) shows a state in which an error is generated in the acquired data by ~~a~~ the jitter.

(28) The paragraph from page 23, line 12 to page 23, line 15 has been amended as follows:

Preferable embodiments of ~~a~~ test equipment, jitter analyzer, and phase difference detector for an LSI to be measured according to the present invention will be described hereinafter with reference to the drawings.

(29) The paragraph from page 24, line 7 to page 24, line 14 has been amended as follows:

The LSI to be measured inputs a signal from a pattern generation unit or the like (not shown) to output predetermined output data, and also outputs a clock signal. As the LSI which outputs the clock by itself, for example, there is an LSI using the technology called "RapidIO" (registered trademark), "HyperTranport" (registered trademark) or the like, a bridge LSI for converting a bus system to "RapidIO" from a PCI bus or the like.

(30) The paragraph from page 30, line 23 to page 30, line 29 has been amended as follows:

Here, information indicating the clock or output data whose signal is input into any channel is usually given beforehand. Therefore, in accordance with the ~~information.~~ information, the operation of the switch to be turned ON/OFF can be set before using the test equipment. This ON/OFF control information can be written in a register for control (not shown) or the like.

(31) The paragraph from page 31, line 29 to page 32, line 9 has been amended as follows:

First, when a predetermined test pattern signal is input into the LSI to be measured 1 from a pattern generation unit (not shown) disposed in the test equipment, ~~predetermined~~ output data and clock corresponding to a pattern signal are output from the LSI to be measured 1. The clock and output data ~~output~~ from the LSI to be measured 1 are input into

separate channels (LSI testers 10). The clock and output data input into each LSI tester 10 are input into the level comparator 11, level-compared with a comparison voltage, and thereafter input into each time interpolator 20.

(32) The paragraph from page 33, line 24 to page 33, line 25 has been amended as follows:

A concrete example will be described hereinafter with reference to ~~FIG. 2~~ FIGS. 2(a) and 2(b).

(33) The paragraph from page 33, line 26 to page 33, line 29 has been amended as follows:

~~FIG. 2 is a signal diagram~~ FIGS. 2(a) and 2(b) are signal diagrams showing an operation for acquiring output data at an edge timing of a clock of the LSI to be measured 1 in the test equipment of the present embodiment.

(34) The paragraph from page 34, line 28 to page 34, line 29 has been amended as follows:

~~A flow of~~ The relationship among the above-described data is ~~shown~~ summarized in Table 1.

(35) The paragraph from page 35, line 17 to page 36, line 2 has been amended as follows:

On the other hand, in the output data, for example, level data "0011" ("H" from the position of bit number "2") is acquired by the flip flops 21a to 21d of the output data side LSI tester 10, and the data is input into each input terminal of the selector 30. In the selector 30 on the output data

side, the data of the input terminal corresponding to bit number "3" is selected by the selection signal input from the clock side and, as a result, the data output from the selector 30 is "H" in the same manner as in FIG. 2(a). ~~A flow of~~ The relationship among the above-described data is ~~shown~~ summarized in Table 2.

(36) The paragraph from page 36, line 5 to page 36, line 16 has been amended as follows:

Therefore, both in FIGS. 2(a) and 2(b), the signal change point fluctuates by the jitter, but the output data "H" is acquired as the data to be measured in either case. When this ~~is acquired in~~ situation is tested by the conventional test equipment of the fixed strobe, "H" is acquired in FIG. 2(a), "L" is acquired in FIG. 2(b), and the data to be measured is not constant (see FIG. 11). Even when the signal change points (edge timings) of the clock and output data of the LSI to be measured 1 fluctuate by the jitter in this manner in the test equipment of the present embodiment, the same result can be constantly acquired in a case where the clock and output data shift ~~in~~ by the same phase.

(37) The paragraph from page 38, line 3 to page 38, line 11 has been amended as follows:

Moreover, since the clock or output data of the LSI to be measured 1 can be allocated to the optional channel in this manner, it is possible to acquire optional output data at the

optional timing of the clock in a case where a plurality of clocks or output data are output from the LSI to be measured 1. Accordingly, in the present embodiment, ~~a~~ highly convenient and versatile test equipment capable of coping with any LSI can be realized.

(38) The paragraph from page 40, line 21 to page 41, line 7 has been amended as follows:

As shown in FIG. 4, the LSI tester 10 (first LSI tester of the present invention) disposed in the jitter analyzer of the present embodiment is a source synchronous circuit including jitter distribution analysis means for inputting the level data of the time series output from the time interpolator 20 to acquire the edge timing of the clock or output data ~~output~~ from the LSI to be measured 1 and for outputting the distribution of jitters of the clock or output data. Concretely, as the jitter distribution analysis means, the storage circuit 50 is disposed to store the timing data output from the encoder 23 of the LSI tester 10. Moreover, a plurality of clocks or output data are acquired from the LSI tester 10 to store a plurality of level data in the storage circuit 50, and ~~a~~ distribution of edge timings of the clock or output data of the LSI to be measured is acquired from the stored data.

(39) The paragraph from page 44, line 8 to page 44, line 16 has been amended as follows:

Concretely, ~~a~~ distribution of edge timings of the clock or output data is acquired as follows. For example, when the clock (or the output data) output from the LSI to be measured 1 is acquired and analyzed as the level data of 4 bits in the same manner as in the signal shown in ~~FIG. 2~~ FIGS. 2(a) and 2(b), the edge timing to change the clock (or the output data) output from the LSI to be measured 1 to "H" from "L" fluctuates between positions of bit numbers "0" and "3".

(40) The paragraph from page 44, line 17 to page 44, line 19 has been amended as follows:

When the signal is processed by the LSI tester 10 of the present embodiment, the flip flops 21a to 21n, and ~~encoders~~ the encoder 23 and the decoder 70 acquire data as follows.

(41) The paragraph from page 48, line 23 to page 48, line 26 has been amended as follows:

A concrete operation of the phase difference detector for the LSI to be measured according to the present embodiment will be described hereinafter with reference to ~~FIG. 8~~ FIGS. 8(a) and 8(b).

(42) The paragraph from page 48, line 27 to page 49, line 1 has been amended as follows:

~~FIG. 8 is a signal diagram~~ FIGS. 8(a) and 8(b) are signal diagrams showing an operation for acquiring a phase difference between the clock and output data of the LSI to be measured in

the phase difference detector for the LSI to be measured according to the present embodiment.

(43) The paragraph from page 53, line 9 to page 53, line 10 has been amended as follows:

The data shown in ~~FIG. 8~~ FIGS. 8(a) and 8(b) will be concretely described hereinafter as an example.

(44) The paragraph from page 53, line 28 to page 53, line 29 has been amended as follows:

~~A concrete flow of~~ The relationship among the data is shown in Tables 4 and 5 as follows.

(45) The paragraph from page 54, line 10 to page 55, line 6 has been amended as follows:

As shown in Tables 4 and 5, in the data output from the decoder 70, only the output terminal indicating the phase difference between the clock and output data of the LSI to be measured 1 indicates "H", and the other output terminals indicate "L". Therefore, "counter output" shows a total of continuously acquired data of FIGS. 8(a) and 8(b), and as a result of data acquisition twice, Table 5 shows a result of one counted phase difference "-1" and one counted phase difference "2". Accordingly, when the output signals of the decoder 70 are counted for each output terminal of the decoder 70 by a plurality of counters 80a to 80n, ~~a~~ distribution of phase differences between the clock and output data of the LSI to be measured 1 can be acquired.

(46) The paragraph from page 56, line 1 to page 56, line 1 has been amended as follows:

~~Industrial Applicability~~

(47) The paragraph from page 56, line 2 to page 56, line 10 has been amended as follows:

As described above, according to ~~a~~ test equipment for an LSI as a device under test of the present invention, a source synchronous circuit is disposed which outputs a clock and output data ~~output~~ from the LSI to be measured as level data in a time series, accordingly a clock signal output from the LSI to be measured is usable as a timing signal to acquire output data of the LSI to be measured, and it is possible to take in the output data at a signal change point synchronized with a jitter.

(48) The paragraph from page 56, line 11 to page 56, line 17 has been amended as follows:

Accordingly, ~~a~~ test equipment for an LSI to be measured can be realized which is capable of obtaining a correct test result without being influenced by the jitter of the output data of the LSI to be measured and which is suitable, for example, for a function test of a high-rate LSI having a data rate exceeding, for example, 1 GHz.